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TMCP700
Transition Module
Installation and Use

TMCP700A/IH1

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Preface

The *TMCP700 Installation and Use* describes the installation, components, and configurations of the main board. The document should be used by anyone who wants general as well as technical information about the TMCP700 products.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

Printed in the United States of America
December 1997

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

Warning

This equipment generates, uses, and can radiate electro-magnetic energy. It may cause or be susceptible to electro-magnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 (CISPR 22) Radio Frequency Interference, Class B

EN50082-1 (IEC801-2, IEC801-3, IEC801-4) Electromagnetic Immunity

The product also fulfills EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

Contents

Figures

Tables

General Information 1

Introduction

This manual provides general information, hardware preparation, installation instructions, and a functional description for the TMCP700-001 Transition Modules.

Product Overview

The TMCP700-001 Transition Module provides the interface between the MCP750-1xxx (hereafter referred to as MCP750) CompactPCI Single Board Computer and various peripheral devices. This module provides industry standard connector access to the IEEE 1284 parallel port, a single mouse/keyboard connector, two RJ-45 connectors providing access to the asynchronous serial ports configured as EIA DTE, and two HD-26 connectors providing access to the serial ports. These serial ports, labeled as Serial 3 and Serial 4 on the face plate of the TMCP700, are individually user configured as EIA-232, EIA-530, V.35, or X.21 DCE or DTE requiring the installation of Motorola's Serial Interface Modules (SIMs).

Features

The features of the TMCP700 Transition Module include:

- Industry-standard connectors for these interfaces:
  - Two asynchronous serial ports (DTE)
  - Two asynchronous/synchronous serial ports, which can be configured for EIA-232-D, EIA-530, V.35, or X.21 interfaces (DCE or DTE)
  - One parallel port (IEEE Standard 1284-I compliant)

  - One combination keyboard/mouse port
- Two 60-pin Serial Interface Module (SIM) connectors for configuring the asynchronous/synchronous serial ports
- One 40-pin header for EIDE port
- One 34-pin header for floppy port
- Two 64-pin headers for PMCIO (1 ground pin provided with each PMCIO signal)
- Single-width board
- Electro-Magnetic Interference (EMI) and Electro-Static Discharge (ESD) protection

General Description

The TMCP700 Transition Module provides the interface between the standard Parallel Port, EIDE port, floppy port, keyboard/mouse port, and the Serial Port connectors, and the MCP750 CompactPCI Single Board Computer module.

All port I/O controllers reside on the Single Board Computer modules. All port circuitry on the transition module is passive, except for Serial ports 3 and 4. The Serial port 3 and 4 circuitry provides multiplexing and buffering functions (refer to *Signal Multiplexing (MX)* on page 3-3). The multiplexing function is transparent to the user.

All MCP750 models use the same transition module.

Figure 1-1 shows the TMCP700 transition module component layout and the front panel. See Table 1-2 for a list of the front panel port connectors.

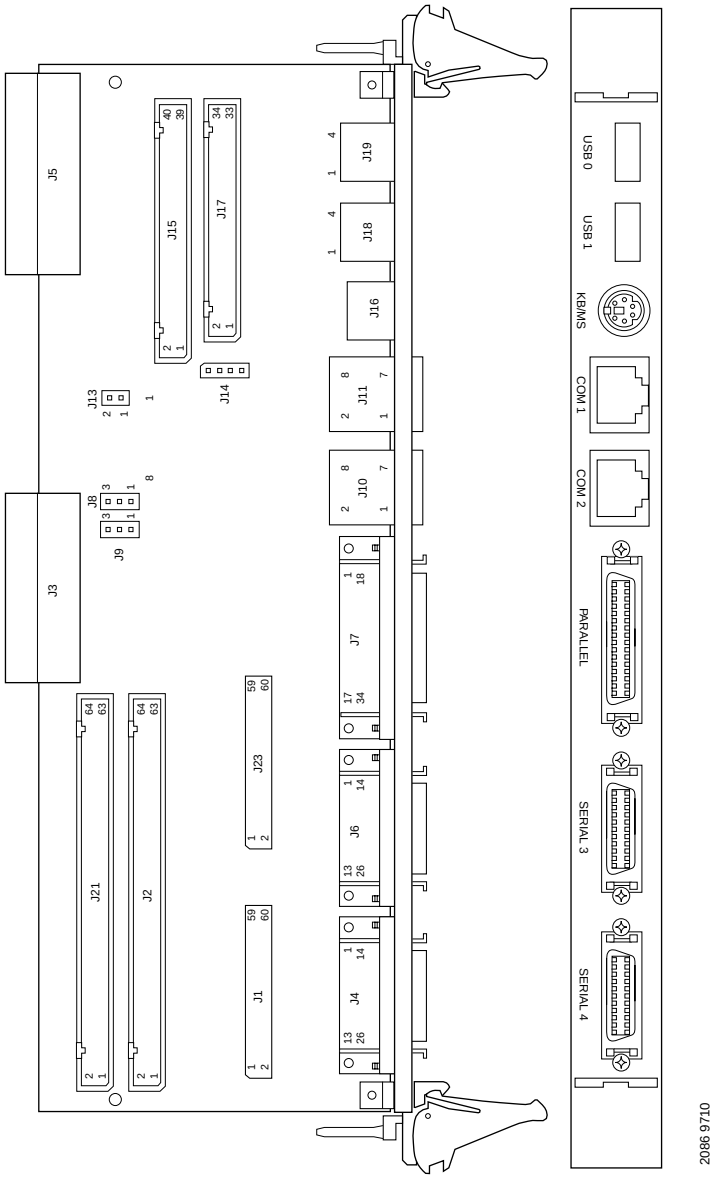


Figure 1-1. TMCP700 Transition Module Front Panel and Component Side

Serial Port Interface Modules

You may configure the asynchronous/synchronous serial ports (Ports 3 and 4) to the appropriate interface by installing a Serial Interface Module (SIM). A SIM is a small "plug-in" printed circuit board that converts the TTL-level synchronous or asynchronous port signals to industry standard voltage levels used by the ports. The SIM contains the receiver and transmitter circuits for converting the input and output signals of the host MCP750 to the appropriate serial data communication protocol.

The SIMs for the TMCP700 are listed in Table 1-1.

Table 1-1. SIM Part Numbers

Interface	Model Number	Part Number
EIA-232-D DCE	SIM232DCE	01-W3876B01B
EIA-232-D DTE	SIM232DTE	01-W3877B01A
EIA-530 DCE	SIM530DCE	01-W3878B01B
EIA-530 DTE	SIM530DTE	01-W3879B01B
V.35 DCE	SIMV35DCE	01-W3128F01A
V.35 DTE	SIMV35DTE	01-W3127F01A
X.21 DCE	SIMX21DCE	01-W3167F01B
X.21 DTE	SIMX21DTE	01-W3166F01A

Note Additional SIMs may be released. Please see your Motorola representative for a complete list of SIMS that are available for the TMCP700.

Connectors and Cables

The connectors on the TMCP700 transition module are listed in Table 1-2. The port connectors are located on the front panel and the top side of the transition module, which is shown in Figure 1-1. Refer to Table 1-3 for a list of the cables and Chapter 4 for the connector pin assignments.

Table 1-2. TMCP700 Transition Module Connectors

Type	Number	Description
COMM 1 and COMM 2	J11 and J10	8-pin female RJ-45 DIN asynchronous serial port connector
Serial Ports 3 and 4	J6 and J4	26-pin female HD-26 synchronous serial port connector
Parallel Port	J7	36-pin female parallel port connector
SIM	J1, J23	60-pin male connector
CompactPCI	J3	95-pin female connector for MCP750 I/O
CompactPCI	J5	110-pin female connector for MCP750 I/O
USB0 & USB1	J19, J18	4-pin USB Series A receptacles (optional)
Keyboard/ Mouse	J16	6-pin circular DIN for combined keyboard/mouse
EIDE	J15	40-pin header for secondary EIDE port
Floppy	J17	34-pin header for floppy port
Speaker	J13	2-pin header for speaker output
PMCIO	J2, J21	Two 64-pin headers for PMCIO (1 ground provided with each PMCIO signal)

Table 1-3. TMCP700 Transition Module Cables

Part Number	Description
User-supplied	EIA-232-D DTE or DCE cable
User-supplied	Centronics-type parallel printer cable, male-to-male
User-supplied	20-conductor cable; usually supplied with the modem
User-supplied	6-conductor cable; usually supplied with the modem
MVME705CBL-001	Straight-through adapter cable to attach a V.35 male connector to an HD-26 female connector, 15 feet long.
MVME705CBL-002	Straight-through adapter cable to attach a V.35 female connector to an HD-26 male connector, 15 feet long.
Supplied with TMCP700	Keyboard/mouse Y-adapter cable (Motorola Part Number 30-W2309E01A)
User-supplied	40-line flat ribbon cable with 40-pin header connectors for EIDE drives
User-supplied	34-line flat ribbon cable with 34-pin header connectors for floppy drive
User-supplied	64-line flat ribbon cable with 64-pin header connectors for PMCIO

Part Number	Description
User-supplied	2-line cable with 2-pin header connector for speaker
30-W2771,DO1A	Straight-through adapter cable to attach a DB-25 male connector to an HD-26 female connector, 15 feet long. May be used for EIA-232-D, or in some cases, EIA-530 applications
30-W2771,DO2A	Straight-through adapter cable to attach a DB-25 female connector to an HD-26 male connector, 15 feet long. May be used for EIA-232-D, or in some cases, EIA-530 applications
30-W2059E01A	Straight-through adapter cable to attach a DB-25 female connector to an HD-26 male connector, 12 feet long

Specifications

The TMCP700 transition module specifications are shown in Table 1-4.

Table 1-4. TMCP700 Specifications

Characteristics	Specifications
Power Requirements	+5Vdc, 175mA typical, 250mA maximum +12Vdc, 100mA typical, 200mA maximum (for some of the SIMs) -12Vdc, 100mA (for some of the SIMs)
Operating temperature	0^{o} to 55^{o} C at chassis point of entry of forced air (approximately 5 CFM)
Storage temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 90% (non-condensing)
Board Size (excluding front panel)	Height: 9.187 inches(233.35 mm) Height: 3.200 inches(80.00 mm) Thickness: 0.063 inches (1.60 mm)

Cooling Requirements

The TMCP700 is tested to operate under forced air cooling with an incoming air temperature range of 0 degrees C to 55 degrees C. Adequate cooling can be achieved with air flowing over the module at 5 cubic feet per minute. The exact amount of air flow required for cooling depends on the ambient air temperature and the type, number, and location of modules and other heat sources.

EMC Compliance

The TMCP700 was tested in an EMC-compliant chassis, and meets the requirements for EN55022 Class B equipment. For minimum RF emissions, it is essential that you implement the following conditions:

- Install shielded cables on all external I/O ports
- Connect conductive chassis rails to earth ground to provide a path for connecting shields to earth ground
- Tighten all front panel screws

1 Specifications

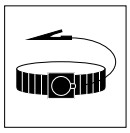
Hardware Preparation and Installation 2

Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the TMCP700 transition module, and the Serial Interface Modules.

Unpacking the Hardware

Use ESD



Wrist Strap

The TMCP700 is packed in an anti-static wrapper to protect it from static discharge. Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when handling the equipment. Electronic components can be extremely sensitive to electro-static discharge (ESD). After removing the board from the protective wrapper, place it component side up on a grounded, static-free surface. Do not slide the board over any surface.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of the equipment.

2

Installing the Serial Interface Modules

Configure the serial ports 3 and 4 for the required interface by installing the appropriate SIM. See "Serial Port Interface Modules" in Section 1 for a list of the serial port interface types.

Prior to installing the SIMs, set the jumpers on header J8 (for Serial Port 3) and header J9 (for Serial Port 4) for either DCE or DTE. Set the jumper to position 1-2 if the SIM is for a DTE interface. Set the jumper to position 2-3 if the SIM is for a DCE interface.

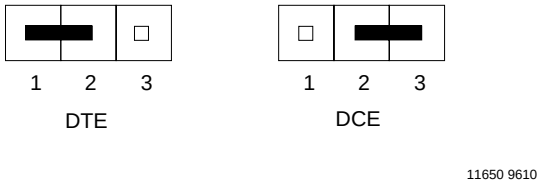


Figure 2-1. Serial Port Interface Jumper Settings

Note You must set the jumpers and install the SIMs prior to installing the TMCP700 transition module in the system chassis.

The SIMs plug into connector J23 (for Serial Port 3) or J1 (for Serial Port 4) on the TMCP700 transition module.

Install the SIMs on the TMCP700 transition module per the following procedure:

1. Align the SIM so that P1 on the SIM lines up with the appropriate SIM connector (J23 for Serial Port 3 or J1 for Serial Port 4) on the transition module. Note the position of the alignment key on P1. See Figure 2-2.
2. Place the SIM onto the transition module SIM connector, making sure that the mounting holes also line up with the standoffs on the transition module as shown in Figure 2-3.

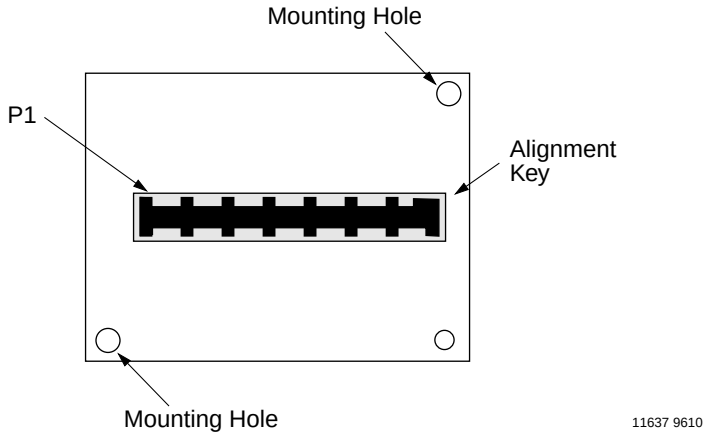


Figure 2-2. Serial Interface Module and Connector P1

3. Gently press the top of the SIM to seat it on the transition module SIM connector. If the SIM does not seat with gentle pressure, re-check the alignment of the connectors.

Note Do not force the SIM onto the transition module.

4. Secure the SIM to the transition module standoffs with the two Phillips-head screws provided. Do not over tighten the screws.

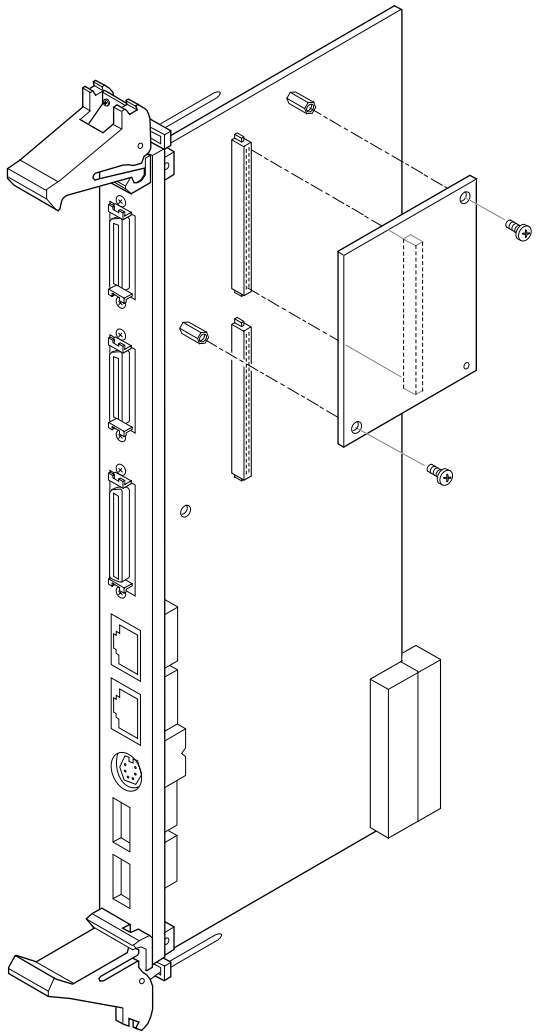
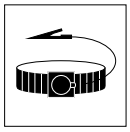


Figure 2-3. Installing a SIM onto the TMCP700 Transition Module

Installing the Transition Module

Installation of the TMCP700 transition module is accomplished from the rear of the system chassis. Any rear panel must be removed in order to see the backplane and install the transition module.

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing boards in a system chassis. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. Place the board flat on a grounded, static-free surface, component-side up. Do not slide the board over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by attaching the ESD wrist strap to an unpainted metal part of the system chassis.

Install the TMCP700 in the system chassis per the following procedure.

1. Turn all equipment power OFF and disconnect the power cable from the AC power source.

Caution

Connecting modules while power is applied may result in damage to components on the module.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. use extreme caution when handling, testing, and adjusting.

2. Remove the chassis cover per the instructions in the equipment user's manual.
3. If the chassis has a rear card cage, remove the filler panel(s) from the appropriate card slot(s) at the rear of the chassis.

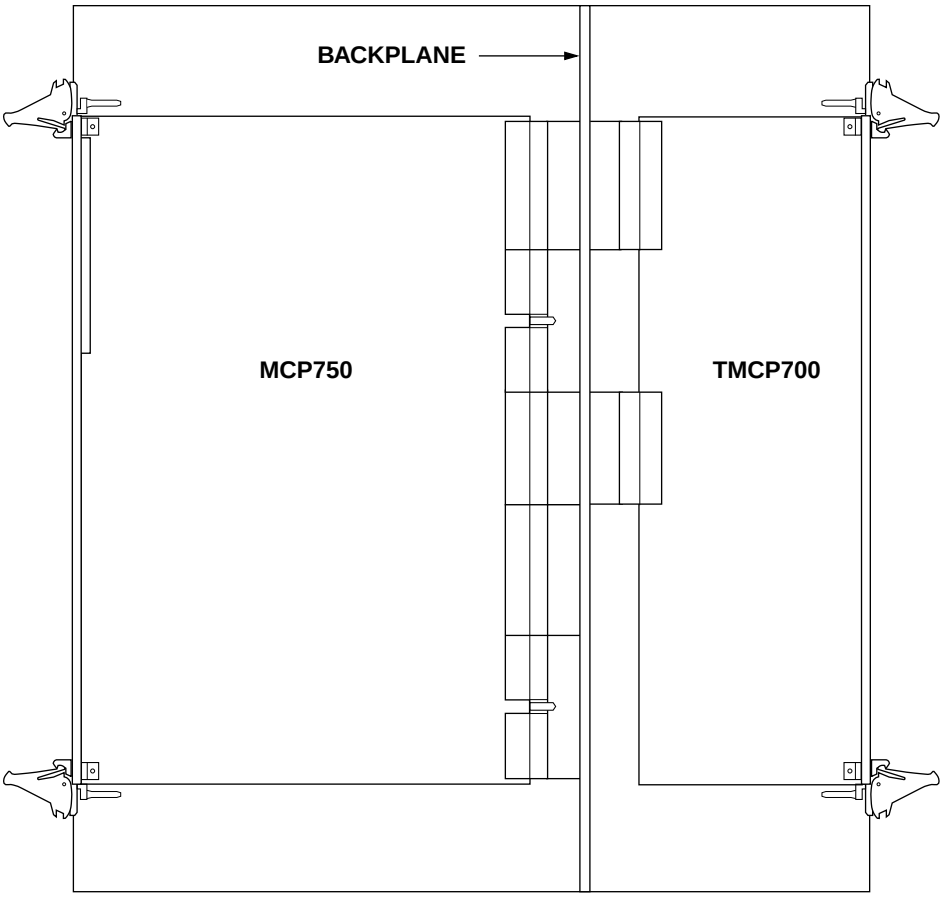


Figure 2-4. TMCP700 Backplane Connections

4. If necessary, move some of the other modules to allow space for the cables connected to the transition module.
5. Install the jumper for Serial ports 3 and 4, if needed (refer to section titled "Installing the Serial Interface Modules."
6. Insert the transition module into the chassis slot making sure the J3/J5 connector pins are properly aligned with the backplane connector pins. Tighten the attaching screws.

Note Make sure there is good contact with the transverse mounting rails in order to minimize RF emissions.

7. Install the chassis cover.

Note Make sure that cables are not pinched by the cover.

8. Connect the power cable to the AC power source.

Functional Description 3

Introduction

This chapter provides information on TMCP700 transition module and SIM circuitry, and the configuration of the serial ports.

Circuitry

The TMCP700 transition module and the Serial Interface Modules (SIMs) convert the TTL level signals to and from the MCP750 module to the reception and transmission levels specified by the appropriate port interface standard.

The TMCP700 transition module contains a small amount of “house keeping” circuitry. Bulk capacitors are on the power sources (+5Vdc, +12Vdc, and -12Vdc). Pullup resistors put the inputs to the MCP750 in a known high even when no SIM is installed.

The block diagram for the TMCP700 transition module is shown in Figure 3-1.

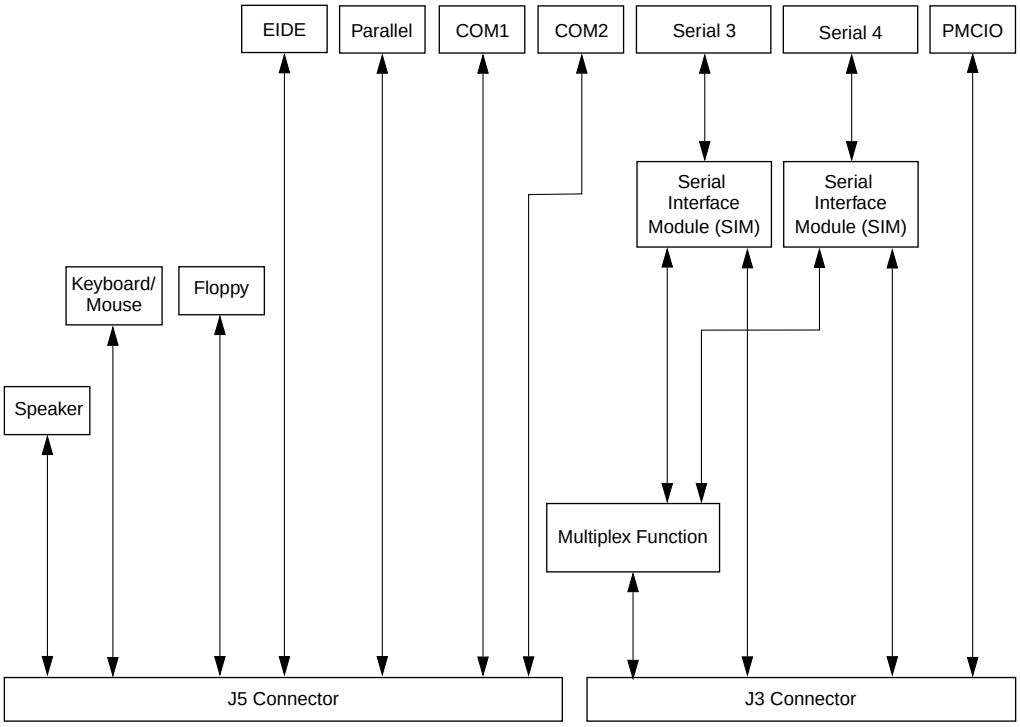


Figure 3-1. TMCP700 Transition Module Block Diagram

Signal Multiplexing (MX)

Because of a limited number of pins on the J3 connector, both the MCP750 processor board and the transition module multiplex and de-multiplex some of the Serial I/O signals. This function, called MX is transparent to the software and the user.

Four pins are used for the signal multiplexing:

- MXCLK
- MXSYNC#
- MXDO
- MXDI

Sixteen Time Slots are defined and allocated. The signal multiplexing sequences are listed in Table 3-1.

Table 3-1. Signal Multiplexing Sequence

MXDO (from the MCP750)		MXDI (from the TMCP700)	
Time Slot	**Signal Name**	**Time Slot**	**Signal Name**
0	RTS3	0	CTS3
1	DTR3	1	DSR3/MID1
2	LLB3/MODSEL	2	DCD3
3	RLB3	3	TM3/MID0
4	RTS4	4	RI3
5	DTR4	5	CTS4
6	LLB4	6	DSR4/MID3
7	RLB4	7	DCD4
8	IDREQ#	8	TM4/MID2
9	Reserved	9	RI4
10	Reserved	10	Reserved
11	Reserved	11	Reserved

Table 3-1. Signal Multiplexing Sequence

MXDO (from the MCP750)		**MXDI (from the TMCP700)**	
12	Reserved	12	Reserved
13	Reserved	13	Reserved
14	Reserved	14	Reserved
15	Reserved	15	Reserved

MXCLK is the 10MHz bit clock for the time-multiplexed data lines, MXDO and MXDI.

MXSYNC# is asserted for one bit time at Time Slot 15 by the MCP750. MXSYNC# is used by the transition module to synchronize with the MCP750.

MXDO is the time-multiplexed output line from the main board and MXDI is the time-multiplexed line from the TMCP700 transition module. A 16-to-1 multiplexing scheme is used with a 10MHz bit rate.

MXSYNC# is clocked out using the falling edge of MXCLK and MXDO is clocked out with the rising edge of the MXCLK. MXDI is sampled at the rising edge of MXCLK (the transition module synchronizes MXDI with MXCLK's rising edge).

The timing relationships among MXCLK, MXSYNC#, MXDO, and MXDI are illustrated in Figure 3-2.

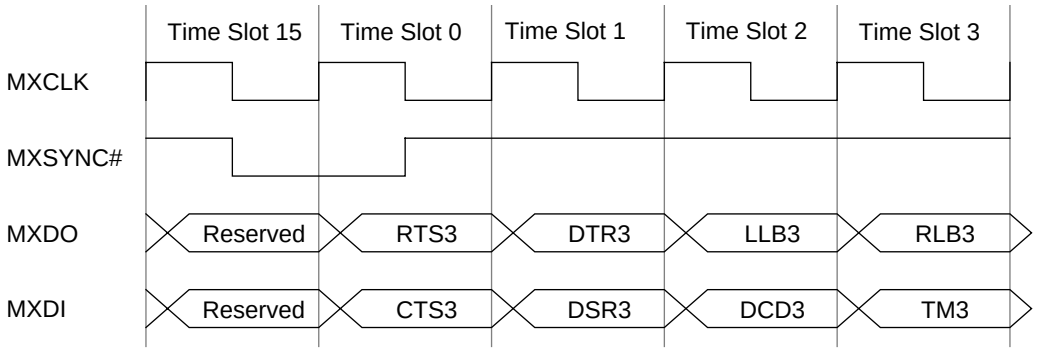


Figure 3-2. Multiplex Signal Timing Chart

Serial Interface Module Circuitry

Each Serial Interface Module has a 60-pin connector that provides all signal and power connections to the TMCP700 transition module.

All TTL-level signals, with the exception of data and clocks, are active low. The pullup resistors on the TMCP700 transition module drive all TTL inputs to the SIM to a known logic level.

The SIMs have surge suppression circuitry for all port signals going to the external connector. This consists of a series resistor and a dual 15V clamp diode to chassis ground. All series resistors are 100 ohms except on the EIA-530 balanced drives, which use 10 ohm series resistors.

The EIA-232-D SIMs employ MC145406 ICs as line transmitters to convert the TTL output signals from the MCP750 module to EIA-232-D voltage levels. As line receivers, the MC145406 ICs convert the EIA-232-D input signals to TTL voltage levels which are sent to the MCP750 module.

The MC145406 transceiver IC requires a series diode on the +12V supply and a clamp diode to logic ground on the -12V supply. The diodes are located on the transition module rather than on the SIM due to space limitations.

The EIA-530 and X.21 SIMs employ AM26C31CD ICs as transmitters to convert the TTL output signals from the MCP750 module to balanced signals. As line receivers, the AM26C32CD ICs convert the balanced input signals to TTL signals which are sent to the MCP750 module.

The V.35 SIMs employ LTC1345T ICs as transmitters to convert the TTL output signals from the MCP750 module to balanced signals. As line receivers, the LTC1345R ICs convert the balanced input signals to TTL signals which are sent to the MCP750 module.

For all port interfaces, the SIMs support the transmitter signal element timing as either input or output signals.

Port Configuration Diagrams

COM1 and COM2 Asynchronous Serial Ports

The asynchronous serial port (COM1 and COM2) configuration is shown in Figure 3-3.

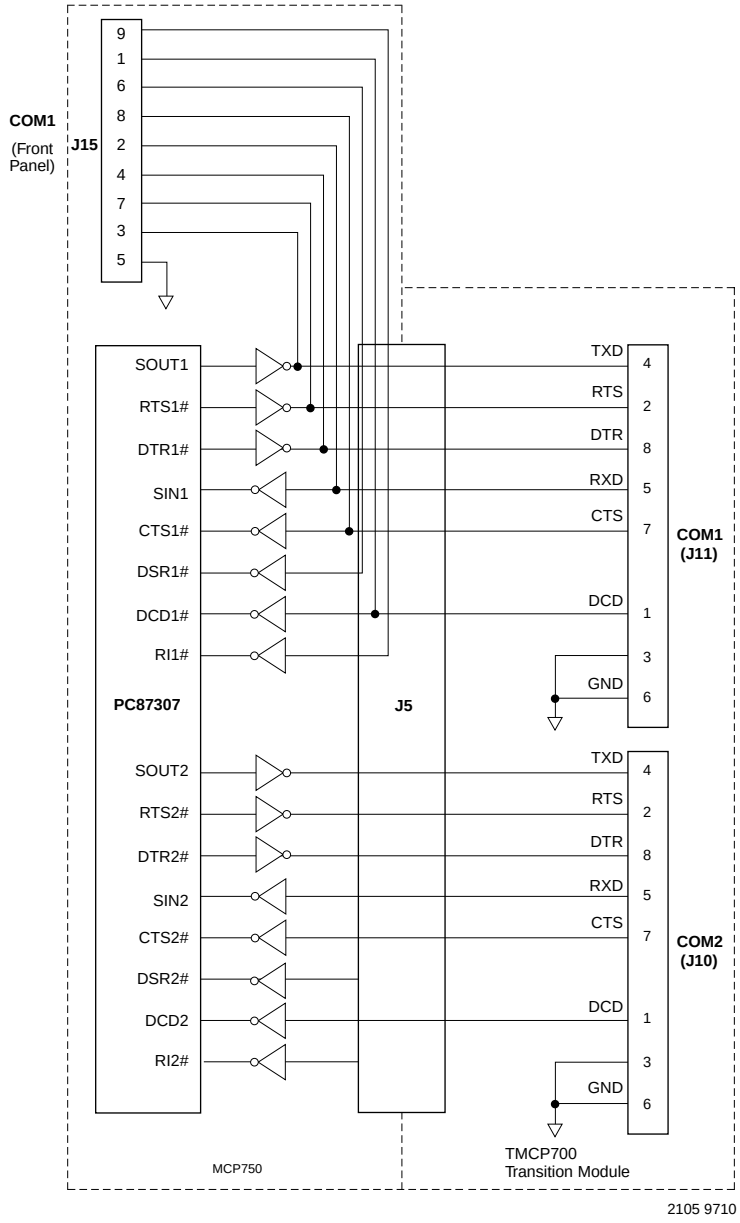


Figure 3-3. DTE Port Configuration (COM1 and COM2)

Asynchronous/Synchronous Serial Ports

The asynchronous/synchronous serial port (Port 3 and Port 4) interface configuration diagrams are on the following pages.

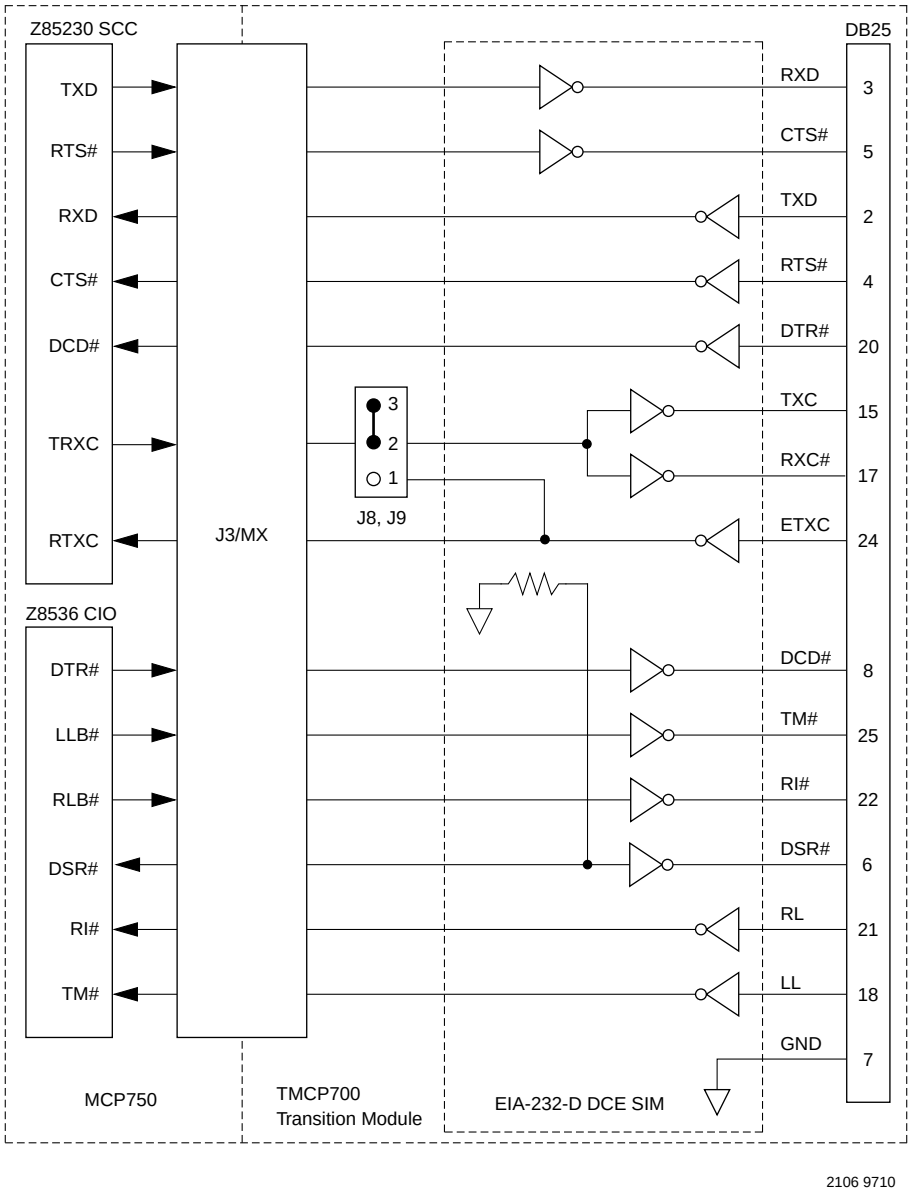


Figure 3-4. EIA-232-D DCE Port Configuration (Ports 3 and 4)

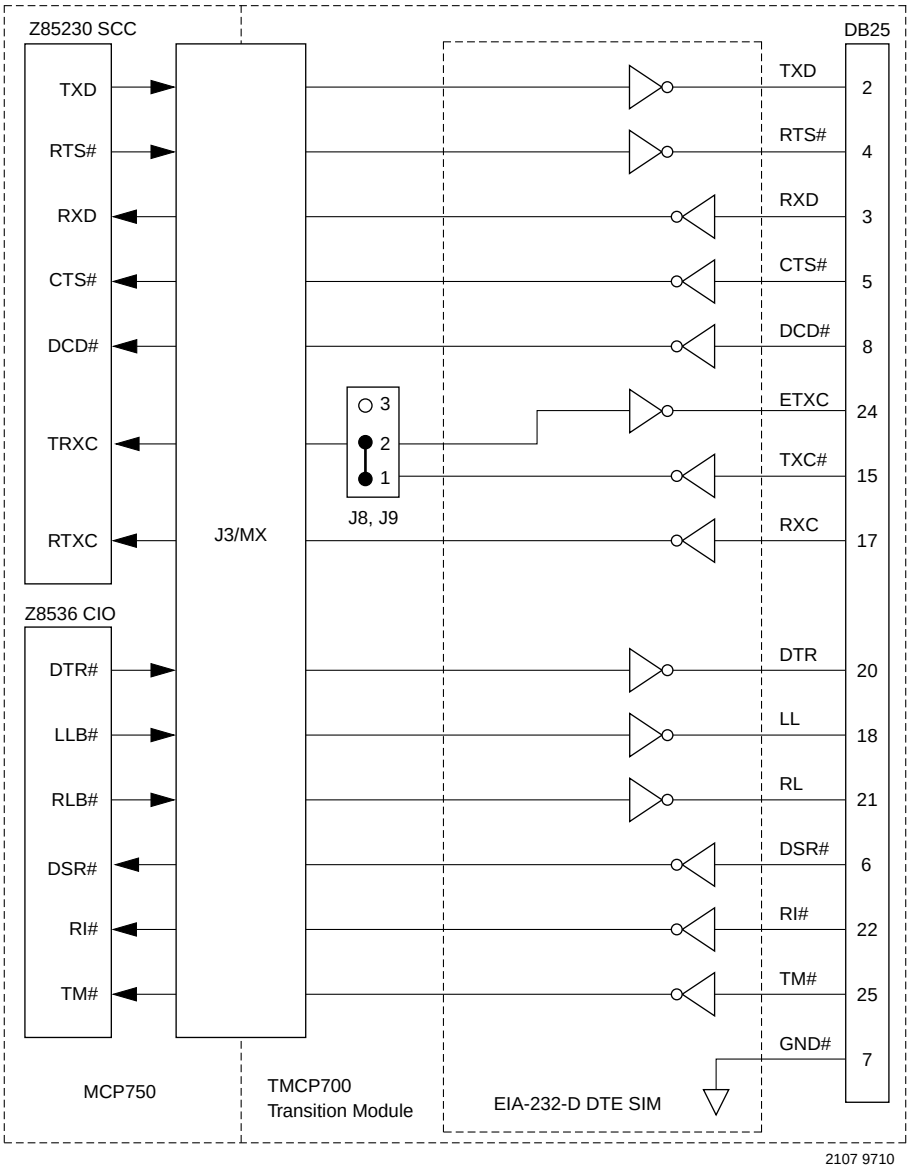


Figure 3-5. EIA-232-D DTE Port Configuration (Ports 3 and 4)

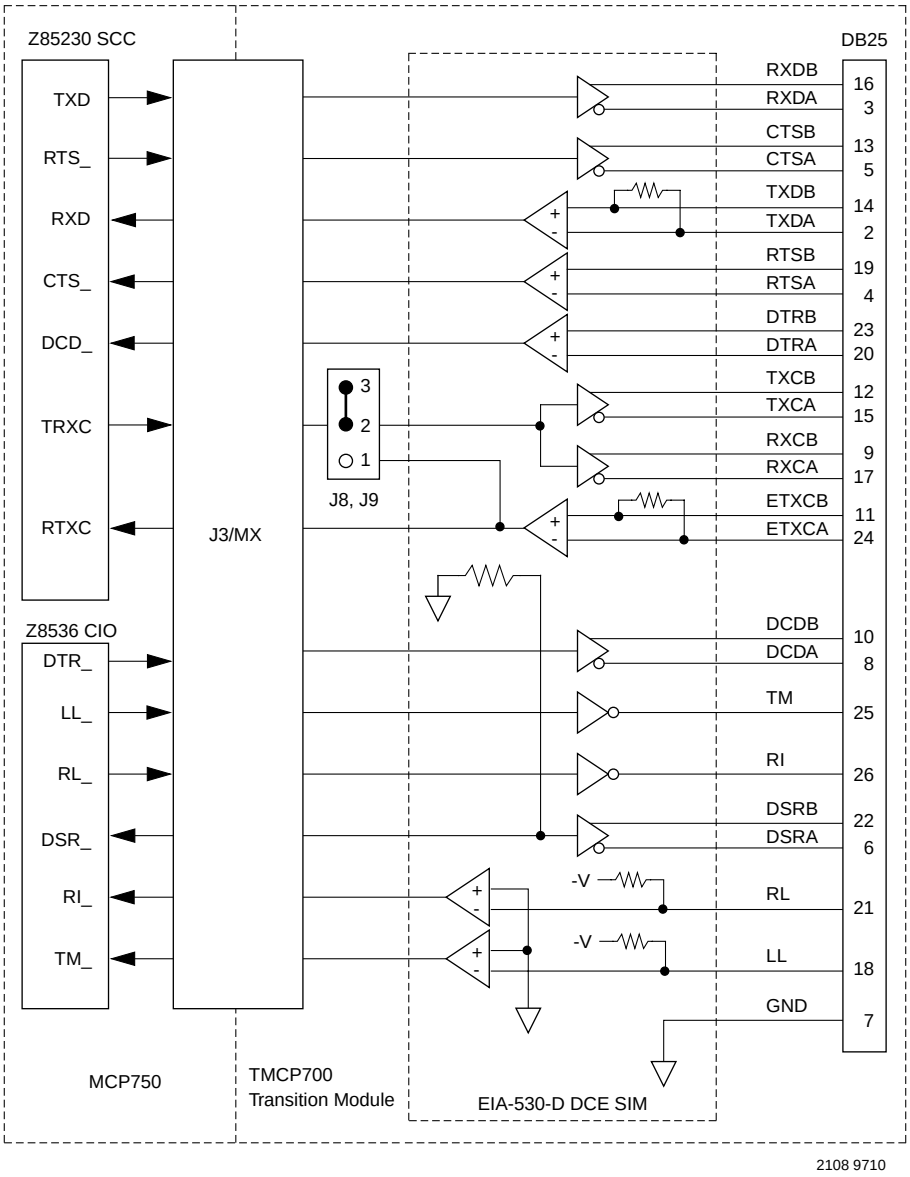


Figure 3-6. EIA-530 DCE Port Configuration (Ports 3 and 4)

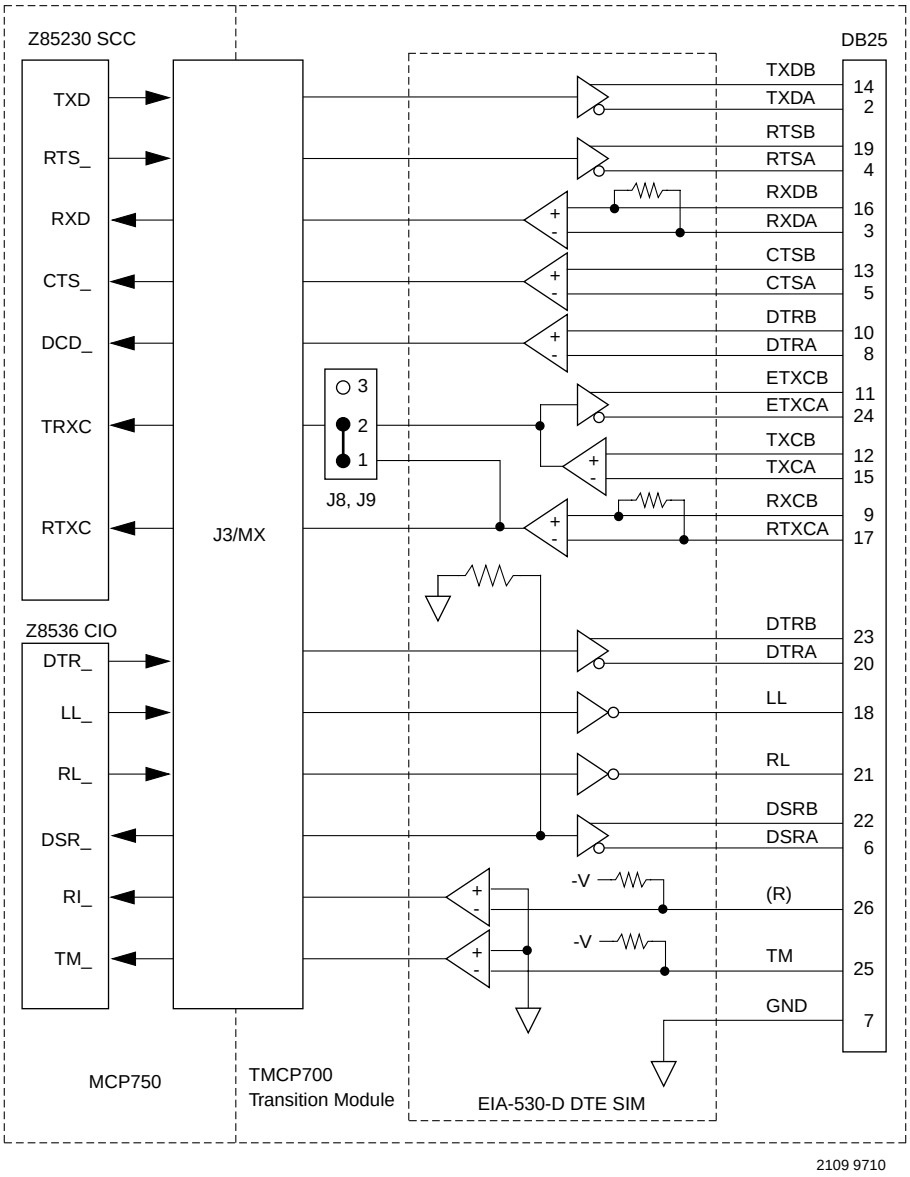


Figure 3-7. EIA-530 DTE Port Configuration (Ports 3 and 4)

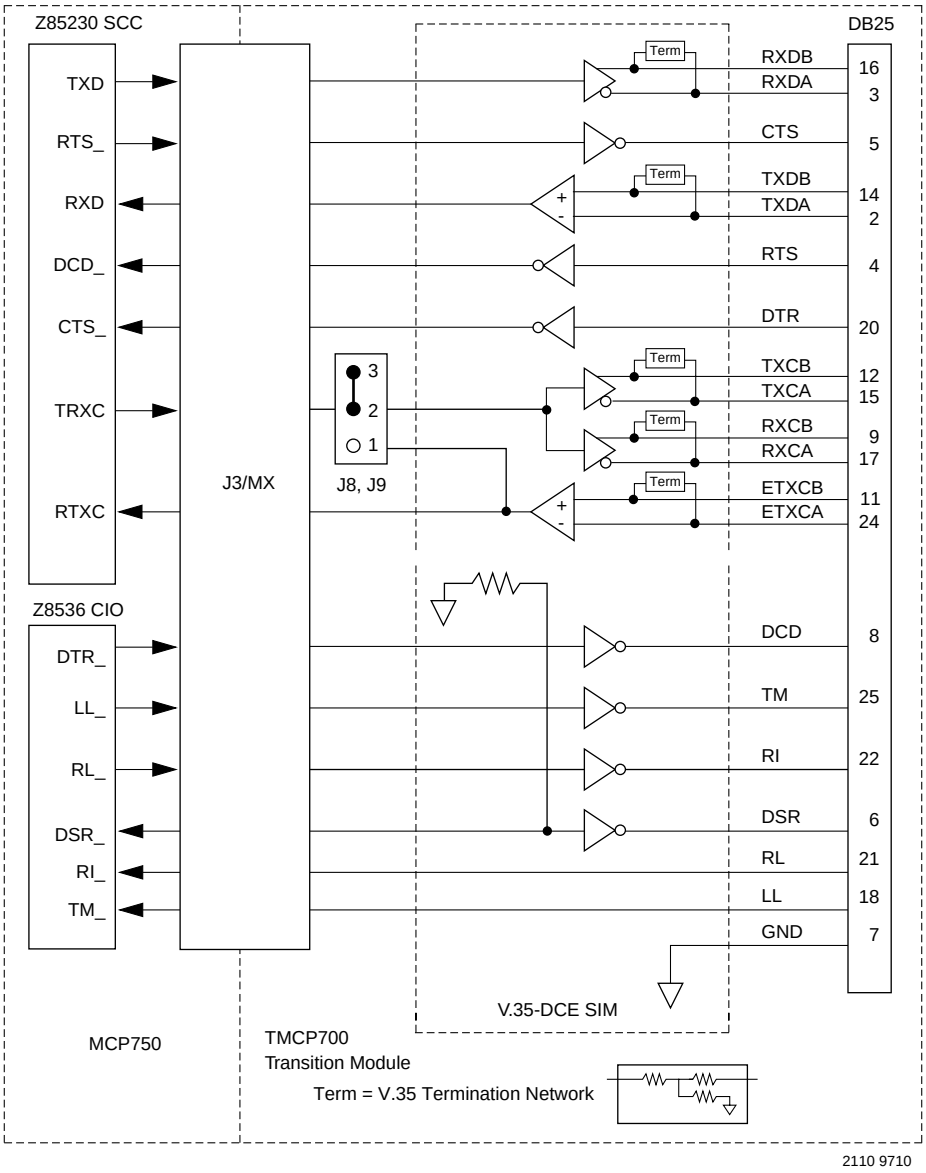


Figure 3-8. V.35-DCE Port Configuration (Ports 3 and 4)

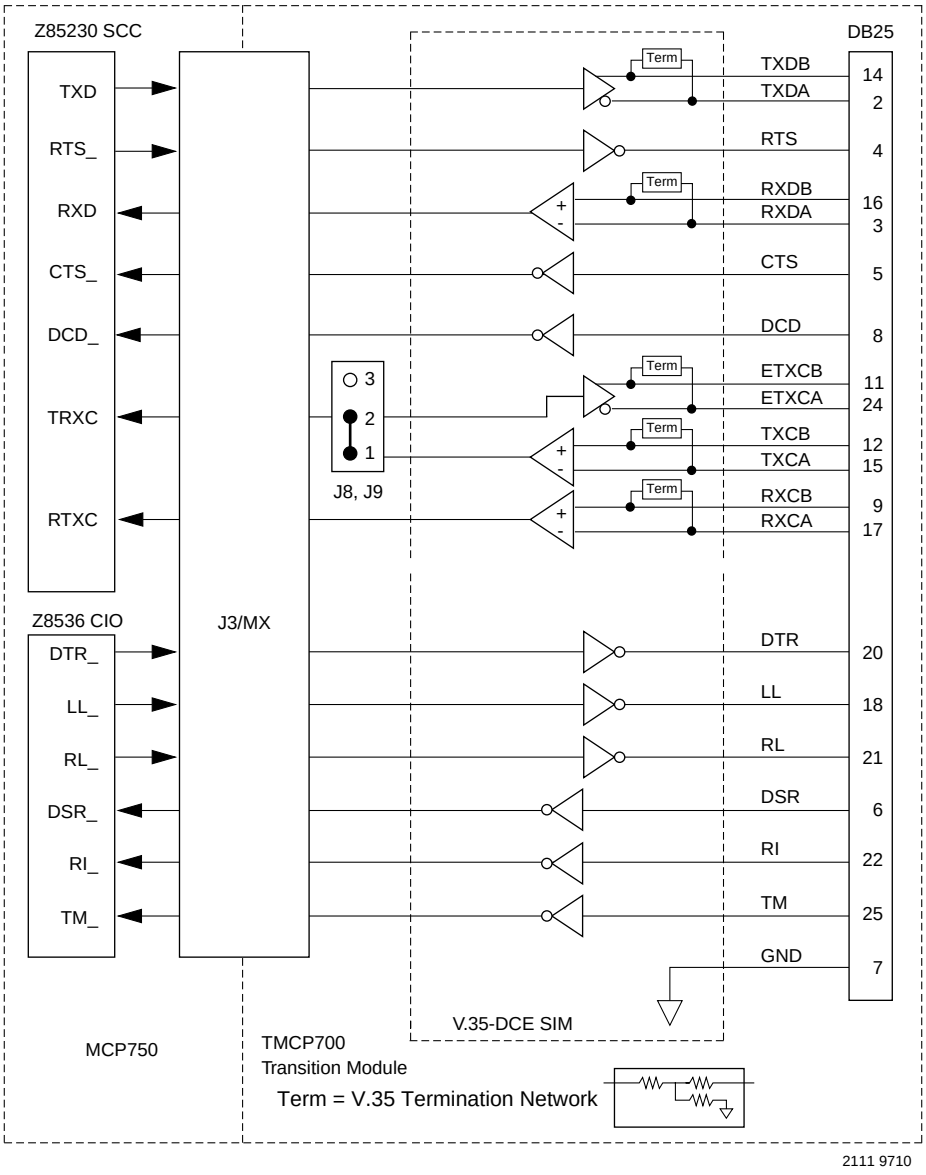


Figure 3-9. V.35-DTE Port Configuration (Ports 3 and 4)

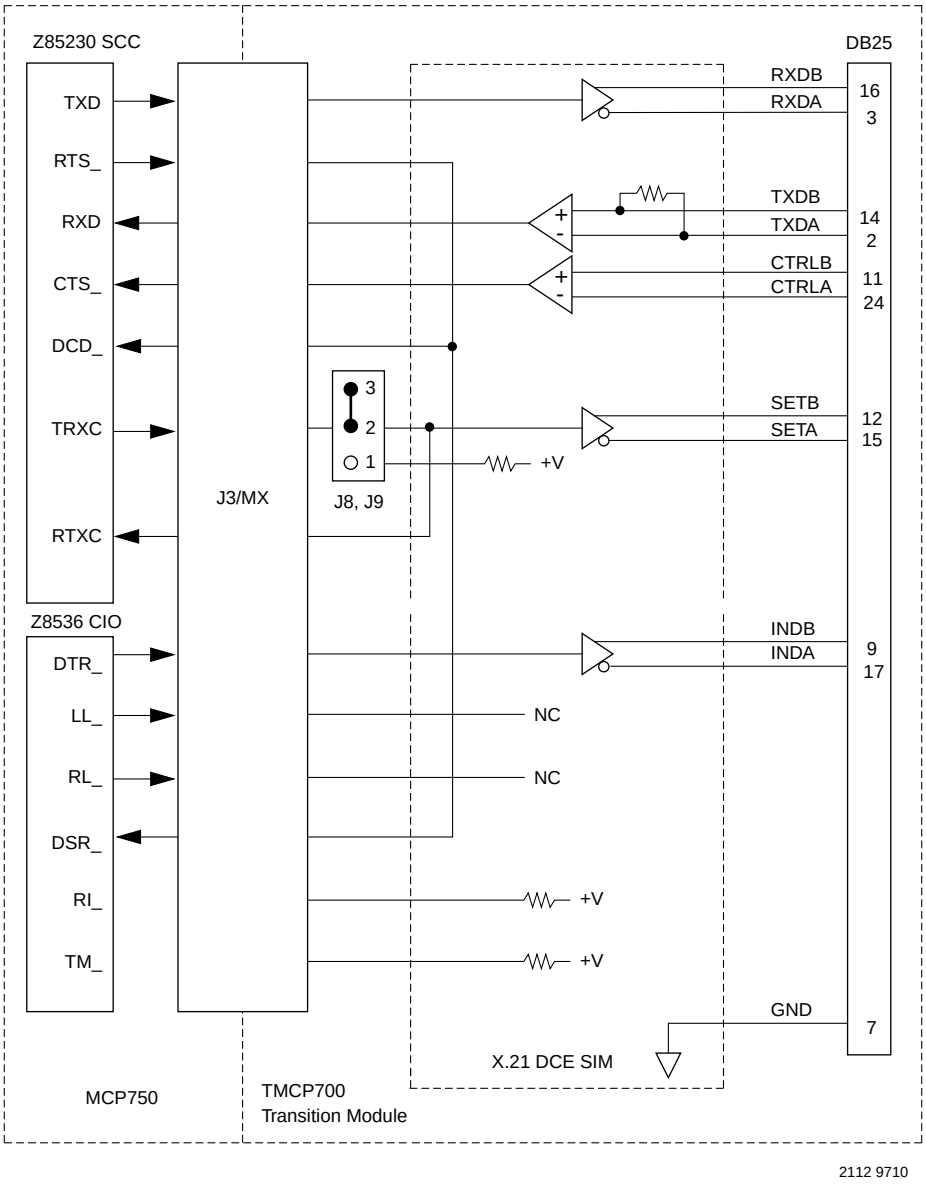


Figure 3-10. X.21-DCE Port Configuration (Ports 3 and 4)

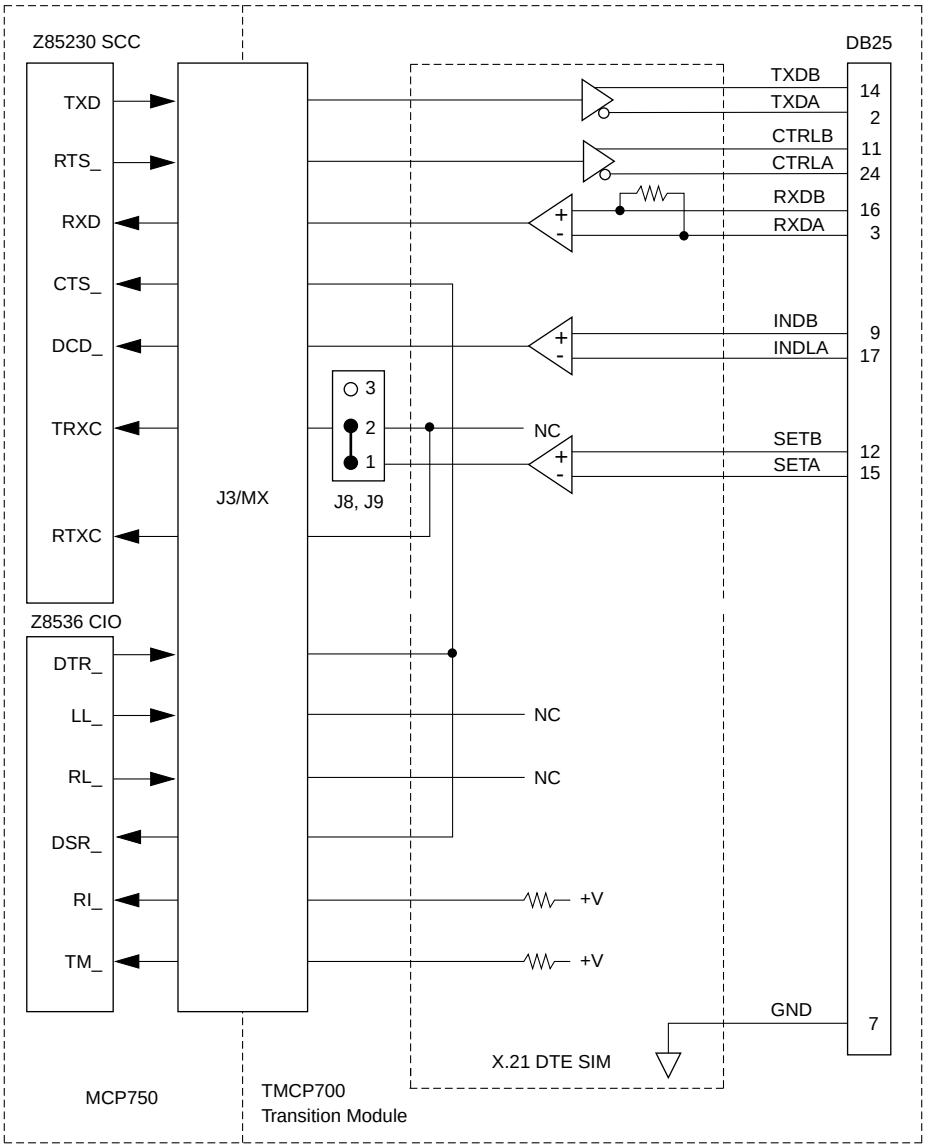


Figure 3-11. X.21-DTE Port Configuration (Ports 3 and 4)

Connector Pin Assignments 4

Introduction

This chapter provides the pin assignments for the J3/J5 connectors and front panel port connectors on the TMCP700 transition module, as well as for the EIDE, floppy, speaker, and PMC I/O connectors.

TMCP700 Transition Module Connectors

J3/J5 Connector

I/O signals and power are provided to the TMCP700 from the MCP750 through CompactPCI connectors J3 and J5.

The pin assignments and signal mnemonics for the TMCP700 transition module connectors are listed in Table 4-1.

CompactPCI User I/O Connector J3

Connector J3 is a 95 pin AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the PMC I/O and serial channels. The pin assignments for J3 are as follows (outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-1: J3 User I/O Connector Pinout

	ROW A	ROW B	ROW C	ROW D	ROW E	
19	Reserved	+12V	-12V	RXD3	RXD4	19
18	Reserved	GND	RXC3	GND	RXC4	18
17	Reserved	MXCLK	MXDI	MXSYNC_L	MXDO	17
16	Reserved	GND	TXC3	GND	TXC4	16
15	Reserved	Reserved	Reserved	TXD3	TXD4	15
14	+3.3V	+3.3V	+3.3V	+5V	+5V	14
13	PMCIO5	PMCIO4	PMCIO3	PMCIO2	PMCIO1	13
12	PMCIO10	PMCIO9	PMCIO8	PMCIO7	PMCIO6	12
11	PMCIO15	PMCIO14	PMCIO13	PMCIO12	PMCIO11	11
10	PMCIO20	PMCIO19	PMCIO18	PMCIO17	PMCIO16	10
9	PMCIO25	PMCIO24	PMCIO23	PMCIO22	PMCIO21	9
8	PMCIO30	PMCIO29	PMCIO28	PMCIO27	PMCIO26	8
7	PMCIO35	PMCIO34	PMCIO33	PMCIO32	PMCIO31	7
6	PMCIO40	PMCIO39	PMCIO38	PMCIO37	PMCIO36	6
5	PMCIO45	PMCIO44	PMCIO43	PMCIO42	PMCIO41	5
4	PMCIO50	PMCIO49	PMCIO48	PMCIO47	PMCIO46	4
3	PMCIO55	PMCIO54	PMCIO53	PMCIO52	PMCIO51	3
2	PMCIO60	PMCIO59	PMCIO58	PMCIO57	PMCIO56	2
1	VIO	PMCIO64	PMCIO63	PMCIO62	PMCIO61	1

User I/O Connector J5

Connector J5 is a 110 pin AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the IDE (secondary port), the keyboard, the mouse, the two USB ports, and the printer ports. The pin assignments for J5 are as follows (the outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-2: J5 User I/O Connector Pinout

	ROW A	ROW B	ROW C	ROW D	ROW E	
22	RESERVED	GND	RESERVED	+5V	SPKROC_L	22
21	KBDDAT	KBDCLK	KBAUXVCC	AUXDAT	AUXCLK	21
20	RESERVED	RESERVED	RESERVED	GND	RESERVED	20
19	STB_L	GND	UVCC0	RESERVED	RESERVED	19
18	AFD_L	RESERVED	RESERVED	GND	UVCC1	18
17	PD2	INIT_L	PD1	ERR_L	PD0	17
16	PD6	PD5	PD4	PD3	SLIN_L	16
15	SLCT	PE	BUSY	ACK_L	PD7	15
14	RTSa	CTSa	RIa	GND	DTRa	14
13	DCDa	+5V	RXDa	DSRa	TXDa	13
12	RTSb	CTSb	RIb	+5V	DTRb	12
11	DCDb	GND	RXDb	DSRb	TXDb	11
10	TR0_L	WPROT_L	RDATA_L	HDSEL_L	DSKCHG_L	10
9	MTR1_L	DIR_L	STEP_L	WDATA_L	WGATE_L	9
8	RESERVED	INDEX_L	MTR0_L	DS1_L	DS0_L	8
7	CS1FX_L	CS3FX_L	DA1	RESERVED	RESERVED	7
6	RESERVED	GND	RESERVED	DA0	DA2	6
5	DMARQ	IORDY	DIOW_L	DMACK_L	DIOR_L	5
4	DD14	DD0	GND	DD15	INTRQ	4
3	DD3	DD12	DD2	DD13	DD1	3
2	DD9	DD5	DD10	DD4	DD11	2
1	RESET_L	DRESET_L	DD7	DD8	DD6	1

Asynchronous Serial Port Connectors

The interface for the asynchronous serial ports, COM1 and COM2, is provided with two RJ-45 connectors, J11 and J10. The connector shields for these ports are tied to chassis ground. The pin assignments and signal mnemonics for these connectors are listed in Table 4-3.

Table 4-3: COM1 (J11) and COM2 (J10) Pin Assignments

Pin	Signal
1	DCD
2	RTS
3	GND
4	TXD
5	RXD
6	GND
7	CTS
8	DTR

Asynchronous/Synchronous Serial Port Connectors

The interface for the asynchronous/synchronous serial ports 3 and 4 is provided by two HD-26 connectors, J6 and J4. The connector shields for these ports are tied to chassis ground.

The pin assignments and signal mnemonics for Serial Port 3 are listed in Table 4-4, and the pin assignments and signal mnemonics for Serial Port 4 are listed in Table 4-5.

Table 4-4: Serial Port 3 (J6) Pin Assignments

Pin	Signal
1	No Connect
2	TXD3
3	RXD3
4	RTS3
5	CTS3
6	DSR3
7	GND
8	DCD3
9	SP3_P9
10	SP3_P10
11	SP3_P11
12	SP3_P12
13	SP3_P13
14	SP3_P14
15	TXCI3
16	SP3_P16
17	RXCI3
18	LLB3

Table 4-4: Serial Port 3 (J6) Pin Assignments (Continued)

Pin	Signal
19	SP3_P19
20	DTR3
21	RLB3
22	RI3
23	SP3_P23
24	TXCO3
25	TM3
26	SP3_P26

Table 4-5: Serial Port 4 (J4) Pin Assignments

Pin	Signal
1	No Connect
2	TXD4
3	RXD4
4	RTS4
5	CTS4
6	DSR4
7	GND
8	DCD4
9	SP4_P9
10	SP4_P10
11	SP4_P11
12	SP4_P12
13	SP4_P13
14	SP4_P14

Table 4-5: Serial Port 4 (J4) Pin Assignments (Continued)

Pin	Signal
15	TXCI4
16	SP4_P16
17	RXCI4
18	LLB4
19	SP4_P19
20	DTR4
21	RLB4
22	RI4
23	SP4_P23
24	TXCO4
25	TM4
26	SP4_P26

Parallel I/O Port Connector

The interface for the parallel port is a standard IEEE P1284-C, 36-pin connector, J7. The functionality of each signal depends on the mode of operation of this bi-directional Parallel Peripheral Interface. Refer to the IEEE P1284 D2.00 Standard for a complete description of each signal function. The connector shield is tied to chassis ground.

The pin assignments and signal mnemonics for this connector are listed in Table 4-6.

Table 4-6: Parallel I/O Connector (J7) Pin Assignments

Pin	Signal	Signal	Pin
1	PRBSY	GND	19
2	PRSEL	GND	20
3	PRACK_	GND	21
4	PRFAULT_	GND	22
5	PRPE	GND	23
6	PRD0	GND	24
7	PRD1	GND	25
8	PRD2	GND	26
9	PRD3	GND	27
10	PRD4	GND	28
11	PRD5	GND	29
12	PRD6	GND	30
13	PRD7	GND	31
14	PRINIT_	GND	32

Table 4-6: Parallel I/O Connector (J7) Pin Assignments (Continued)

Pin	Signal	Signal	Pin
15	PRSTB_	GND	33
16	SELIN_	GND	34
17	AUTOFD_	GND	35
18	Pull-up	No Connect	36

Keyboard/Mouse Connector

The Keyboard / Mouse interface is provided by a 6-pin circular DIN connector. To use the keyboard function only, a keyboard may be connected directly to this connector. To use both the keyboard and the mouse functions, use the Y-adapter cable provided with the TMCP700. Refer to the following table for pin assignments.

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Table 4-7: Keyboard/Mouse Connector (J16) Pin Assignments

Pin	Signal
1	KBD DAT
2	MSDAT
3	GND
4	+5Vdc Fused
5	KBDCLK
6	MSCLK

USB Connectors

The standard version of the MCP750 routes the USB port signals only to the MCP750 front panel USB connectors J18 and J17. Therefore the USB port connectors (J19 and J18) on the TMCP700 are not active. The USB ports can be routed to the TMCP700 using an alternate build option of the MCP750. Contact your local Motorola Sales office for details.

EIDE Connector

The TMCP700 provides a 40-pin header (J15) to interface to the MCP750 secondary EIDE port. The pin assignments and signal mnemonics for this connector are listed below.

Table 4-8: EIDE Connector (J15) Pin Assignments

Pin	Signal	Signal	Pin
1	DRESET_L	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	No Connect	20
21	DMARQ	GND	22
23	DIOW_L	GND	24
25	DIOR_L	GND	26
27	IORDY	No Connect	28
29	DMACK_L	GND	30
31	INTRQ	No Connect	32
33	DA1	No Connect	34
35	DA0	DA2	36
37	CS1FX_L	CS3FX_L	38
39	No Connect	GND	40

Floppy Port Connector

The TMCP700 provides a 34-pin header (J17) to interface to a floppy disk drive. The pin assignments and signal mnemonics for this connector are listed below.

Table 4-9: Floppy Connector (J17) Pin Assignments

Pin	Signal	Signal	Pin
1	GND	No Connect	2
3	GND	No Connect	4
5	GND	No Connect	6
7	No Connect	INDEX_L	8
9	GND	MTR0_L	10
11	GND	DS1_L	12
13	No Connect	DS0_L	14
15	GND	MTR1_L	16
17	No Connect	DIR_L	18
19	GND	STEP_L	20
21	GND	WDATA_L	22
23	GND	WGATE_L	24
25	GND	TR0_L	26
27	GND	WPROT_L	28
29	GND	RDATA_L	30
31	GND	HDSEL_L	32
33	GND	DSKCHG_L	34

+5Vdc Power Connector (J14)

The TMCP700 has a 4-pin header that can be used to provide +5Vdc power to offboard devices. This power is derived from the fused +5Vdc power on the MCP750. Any external device powered from this connector must not draw more than 200mA. The pin assignments are listed in the following table.

Table 4-10: +5Vdc Power Connector (J14)

Pin	Signal
1	+5Vdc
2	GND
3	GND
4	No Connect

Speaker Output Connector (J13)

The 2-pin header (J13) provides connection to an external speaker from the MCP750 PCB Counter 2 output. The speaker driver, located on the MCP750 PCB, consists of a 500 mA (max) current sink transistor in series with a 33 ohm resistor. The pin assignments are listed in the following table.

Table 4-11: Speaker Output Connector (J13)

Pin	Signal
1	GND
2	SPKROC_L

PMC I/O Connectors

The PMC I/O connectors consist of two 64-pin header connectors J2 and J21. The pin assignments and signal mnemonics for these connectors are listed below.

Table 4-12: PMC I/O Connector (J2)

Pin	Signal	Signal	Pin
1	GND	PMCIO1	2
3	GND	PMCIO2	4
5	GND	PMCIO3	6
7	GND	PMCIO4	8
9	GND	PMCIO5	10
11	GND	PMCIO6	12
13	GND	PMCIO7	14
15	GND	PMCIO8	16
17	GND	PMCIO9	18
19	GND	PMCIO10	20
21	GND	PMCIO11	22
23	GND	PMCIO12	24
25	GND	PMCIO13	26
27	GND	PMCIO14	28
29	GND	PMCIO15	30
31	GND	PMCIO16	32
33	GND	PMCIO17	34
35	GND	PMCIO18	36
37	GND	PMCIO19	38
39	GND	PMCIO20	40
41	GND	PMCIO21	42

Table 4-12: PMC I/O Connector (J2)

Pin	Signal	Signal	Pin
43	GND	PMCIO22	44
45	GND	PMCIO23	46
47	GND	PMCIO24	48
49	GND	PMCIO25	50
51	GND	PMCIO26	52
53	GND	PMCIO27	54
55	GND	PMCIO28	56
57	GND	PMCIO29	58
59	GND	PMCIO30	60
61	GND	PMCIO31	62
63	GND	PMCIO32	64

Table 4-13: PMCIO Connector (J21)

Pin	Signal	Signal	Pin
1	GND	PMCIO33	2
3	GND	PMCIO34	4
5	GND	PMCIO35	6
7	GND	PMCIO36	8
9	GND	PMCIO37	10
11	GND	PMCIO38	12
13	GND	PMCIO39	14
15	GND	PMCIO40	16
17	GND	PMCIO41	18
19	GND	PMCIO42	20
21	GND	PMCIO43	22

Table 4-13: PMCIO Connector (J21) (Continued)

Pin	Signal	Signal	Pin
23	GND	PMCIO44	24
25	GND	PMCIO45	26
27	GND	PMCIO46	28
29	GND	PMCIO47	30
31	GND	PMCIO48	32
33	GND	PMCIO49	34
35	GND	PMCIO50	36
37	GND	PMCIO51	38
39	GND	PMCIO52	40
41	GND	PMCIO53	42
43	GND	PMCIO54	44
45	GND	PMCIO55	46
47	GND	PMCIO56	48
49	GND	PMCIO57	50
51	GND	PMCIO58	52
53	GND	PMCIO59	54
55	GND	PMCIO60	56
57	GND	PMCIO61	58
59	GND	PMCIO62	60
61	GND	PMCIO63	62
63	GND	PMCIO64	64

Related Documentation A

Motorola Computer Group Documents

This product ships with an installation and use manual, which includes installation instructions, jumper configuration information, memory maps, debugger/monitor commands, and any other information needed to install and operate the board.

If you plan to develop your own applications or need more detailed information about this product, you may want to order one or more documents listed on the following pages. To order:

- Contact your local Motorola sales office,
- Access the World Wide Web site listed on the back cover of this and other MCG manuals and select "Product Literature", or
- (USA and Canada only) —Contact the Literature Center via phone or fax at the numbers listed under *Product Literature* at MCG's World Wide Web site

Any supplements issued for a specific revision of a manual or guide are furnished with that document. The "type" and "revision level" of a specific manual are indicated by the last three characters of the document number, such as "/IH2" (the second revision of an installation manual); a supplement bears the same number as a manual but has two additional characters that indicate the revision level of the supplement, for example "/IH2A1" (the first supplement to the second edition of the installation manual).

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
MCP750 CompactPCI Single Board Computer Installation and Use	MCP750A/IH1
MCP750 CompactPCI Single Board Computer Programmer's Reference Guide	MCP750A/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual	PPCDIAA/UM

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

To further assist your development effort, Motorola has collected some of the non-Motorola documents in this list from the suppliers. These are listed in Table A-2.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
MPC750^{TM} RISC Microprocessor Technical Summary Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC750/D

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
MPC750™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC750UM/AD MPR604UMU-01
PowerPC™ Microprocessor Family: The Programming Environments Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01
DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-QC0CA-TE

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
DECchip 21154 PCI-to-PCI Bridge Data Sheet Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-R24JA-TE
Digital Semiconductor 21x4 Serial ROM Format, Version 3.03 Specification, May 28, 1996. Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	
PC87307VUL (Super I/O™ Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87307VUL
MK48T559 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T559

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8293-02
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8319-00
VT82C586B PIPC PCI Integrated Peripheral Controller VIA Technologies, Inc. 5020 Brandin Court Fremont, CA 94538 Telephone: (510) 683-3300 FAX: (510) 683-3301	VT82C586B
ATMEL Nonvolatile Memory Data Book Atmel Corporation 2325 Orchord Parkway San Jose, CA 95131 Telephone: (408) 441-0311 FAX: (408) 436-4300 Website: http://www.atmel.com	AT24C04

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 2.0
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St. #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: (800) 282-2732 FAX: (716) 871-6511 OR IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC OR Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRPPCHRP-01 ISBN 1-55860-394-8
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Compact PCI Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	CPCI Rev. 2.1 Dated 9/2/97
PCI-to-PCI Bridge Specification PCI-ISA Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	Rev. 1.02 Rev. 2.0

Glossary

Abbreviations, Acronyms, and Terms to Know

This glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10Base-5 An Ethernet implementation in which the physical medium is a doubly shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet). Also known as thick Ethernet.

10Base-2 An Ethernet implementation in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet). Also known as thin Ethernet.

10Base-T An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters. Also known as twisted-pair Ethernet.

100Base-TX An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 100 Mbps for a maximum distance of 100 meters. Also known as fast Ethernet.

ACIA **A**synchronous **C**ommunications **I**nterface **A**dapter

AIX **A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)

architecture The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.

ASCII **A**merican **S**tandard **C**ode for **I**nformation **I**nterchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8-bits to encode a total of 256 alphanumeric and control characters.

ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
AUI	**A**ttachment **U**nit **I**nterface
BBRAM	Battery Backed-up Random Access Memory
bi-endian	Having big-endian and little-endian byte ordering capability.
big-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.
BIOS	**B**asic **I**nput/**O**utput **S**ystem. This is the built-in program that controls the basic functions of communications between the processor and the I/O (peripherals) devices. Also referred to as ROM BIOS.
BLT	**BL**ock **T**ransfer
board	The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.
bpi	**b**its **p**er **i**nch
bps	**b**its **p**er **s**econd
bus	The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.
cache	A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids accessing the slower hard or floppy disk drive.
CAS	**C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.

CD	**C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.
CD-ROM	**C**ompact **D**isk **R**ead-**O**nly **M**emory
CFM	**C**ubic **F**eet per **M**inute
CHRP	See Common Hardware Reference Platform (CHRP).
CHRP-compliant	See Common Hardware Reference Platform (CHRP).
CHRP Spec	See Common Hardware Reference Platform (CHRP).
CIO	Counter/Timer and Parallel I/O unit (Zilog Z8536).
CISC	**C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.
CODEC	**CO**der/**DEC**oder
Common Hardware Reference Platform (CHRP)	A specification published by the Apple, IBM, and Motorola which defines the devices, interfaces, and data formats that make up a CHRP-compliant system using a PowerPC processor.
CPU	**C**entral **P**rocessing **U**nit. The master computer unit in a system.
DCE	**D**ata **C**ircuit-terminating **E**quipment.
DLL	**D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.
DMA	**D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.
DOS	**D**isk **O**perating **S**ystem
dpi	**d**ots **p**er **i**nch

DRAM	**D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.
DTE	**D**ata **T**erminal **E**quipment.
ECC	**E**rror **C**orrection **C**ode
ECP	**E**xtended **C**apability **P**ort
EEPROM	**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.
EIDE	Enhanced Intelligent Device Expansion
EISA (bus)	**E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of 16-bit or 8-bit that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.
EPP	**E**nhanced **P**arallel **P**ort
EPROM	**E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.
ESCC	**E**nhanced **S**erial **C**ommunication **C**ontroller
ESD	**E**lectro-**S**tatic **D**ischarge/Damage
Ethernet	A local area network standard that uses radio frequency signals carried by coaxial cables.
Falcon	A DRAM controller chip developed by Motorola for a series of PowerPC board level products. It is intended to be used in sets of two to provide the necessary interface between the Power PC60*x* bus and the 144-bit ECC DRAM (system memory array) and/or ROM/Flash.
fast Ethernet	See 100Base-TX.
FDC	**F**loppy **D**isk **C**ontroller

FIFO	**F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.
firmware	The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).
frame	One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.
graphics controller	On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.
HAL	**H**ardware **A**bstraction **L**ayer. The lower level hardware interface module of the Windows NT operating system. It contains platform specific functionality.
hardware	A computing system is normally spoken of as having two major components: hardware and software. Hardware is the term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system.
HCT	**H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.
I/O	**I**nput/**O**utput
IBC	PCI/**I**SA **B**ridge **C**ontroller
IDC	**I**nsulation **D**isplacement **C**onnector
IDE	**I**ntelligent **D**evice **E**xpansion
IEEE	**I**nstitute of **E**lectrical and **E**lectronics **E**ngineers
IQ Signals	Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

ISA (bus)	**I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)
ISASIO	**ISA S**uper **I**nput/**O**utput device
ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.
LAN	**L**ocal **A**rea **N**etwork
LED	**L**ight-**E**mitting **D**iode
LFM	**L**inear **F**eet per **M**inute
little-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.
MBLT	**M**ultiplexed **BL**ock **T**ransfer
MCA (bus)	**M**icro **C**hannel **A**rchitecture
MCG	**M**otorola **C**omputer **G**roup
MFM	**M**odified **F**requency **M**odulation
MIDI	**M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.
MPC	**M**ultimedia **P**ersonal **C**omputer
MPC750	Motorola's component designation for the PowerPC 750 microprocessor.
MPIC	**M**ulti-**P**rocessor **I**nterrupt **C**ontroller
MPU	**M**icro**P**rocessing **U**nit
MTBF	**M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how

	long a device, or any individual device is likely to last, nor is it a warranty, but rather, of the relative reliability of a family of products.
multisession	The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.
nonvolatile memory	A memory in which the data content is maintained whether the power supply is connected or not.
NTSC	**N**ational **T**elevision **S**tandards **C**ommittee (USA)
NVRAM	**N**on-**V**olatile **R**andom **A**ccess **M**emory
OEM	**O**riginal **E**quipment **M**anufacturer
OMPAC	**O**ver - **M**olded **P**ad **A**rray **C**arrier
OS	**O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.
OTP	**O**ne-**T**ime **P**rogrammable
parallel port	A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.
PBC	Peripheral Bus Controller (PCI-to-ISA Bridge)
PCI (local bus)	**P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.
PCMCIA (bus)	**P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.
PCR	**P**CI **C**onfiguration **R**egister
PHB	**P**CI **H**ost **B**ridge
PDS	**P**rocessor **D**irect **S**lot
physical address	A binary address that refers to the actual location of information stored in secondary storage.
PIB	**P**CI-to-**I**SA **B**ridge

PLL	**P**hase-**L**ocked **L**oop
PMC	**P**CI **M**ezzanine **C**ard
POWER	**P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)
PowerPC™	The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.
PowerPC 750™	The fourth implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and a 64KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 750 is used by Motorola, Inc. under license from IBM.
PowerPC Reference Platform (PRP)	A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.
PROM	**P**rogrammable **R**ead-**O**nly **M**emory
PS/2	**P**ersonal **S**ystem/**2** (IBM)
QFP	**Q**uad **F**lat **P**ackage
RAM	**R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.
RAS	**R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Raven The PowerPC-to-PCI local bus bridge chip developed by Motorola for the MVME2600 and MVME3600 series of boards. It provides the necessary interface between the PowerPC 60x bus and the PCI bus, and acts as interrupt controller.

Reduced-Instruction-Set Computer (RISC) A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced Instruction Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC **R**eal-**T**ime **C**lock

SBC **S**ingle **B**oard **C**omputer

SCSI **S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. SCSI-1 provides up to 5 Mbps data transfer.

SCSI-2 (Fast/Wide) An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.

serial port A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.

SIM **S**erial **I**nterface **M**odule

SIMM **S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) on it designed to fit into a standard slot.

SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	A computing system is normally spoken of as having two major components: hardware and software. Software is the term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer
standard(s)	A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.
Teletext	One way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.
thick Ethernet	See 10Base-5.
thin Ethernet	See 10Base-2.
twisted-pair Ethernet	See 10Base-T.
UART	**U**niversal **A**synchronous **R**eceiver/**T**ransmitter
Universe	ASIC developed by Tundra in consultation with Motorola, that provides the complete interface between the PCI bus and the 64-bit VMEbus.
USB	Universal Serial Bus

UV	**U**ltra**V**iolet
VESA (bus)	**V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.
virtual address	A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.
VL bus	See **V**ESA **L**ocal bus (VL bus).
VMEchip2	MCG second generation VMEbus interface ASIC (Motorola)
VME2PCI	MCG ASIC that interfaces between the PCI bus and the VMEchip2 device.
volatile memory	A memory in which the data content is lost when the power supply is disconnected.
VRAM	**V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

GLOSSARY

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